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PAJ 11-01-94 06308204 JP **BOARD TEST SYSTEM**

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PURPOSE: To analyze failures of components or wiring patterns and specify failure positions in the operational state by optically detecting the potentials at individual positions in the circuit test and failure analysis of a mounted board. CONSTITUTION: A voltage detecting sensor 2 fitted with a transparent electrode on the surface of an electro-optical effect material and conductive reflecting film and a soft dielectric substance in the lattice point state on the back face and fitted with it to a transparent support plate is closely stuck to a mounted board, and the position signal and voltage from a laser transceiver 1 and a laser scanning device are detected. They are converted into the potential distribution image of the mounted board by a potential distribution acquiring circuit 4, and the image is stored in a memory 5. Potential distribution images of a good object and a defective object are acquired synchronously with the clock while the mounted board is set to the operational state, a differential image is obtained by a differential image detecting circuit 6, the position where the differential image is first generated is specified, and the failure position is specified. COPYRIGHT: (C)1994,JPO

NO-DESCRIPTORS